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**Notice of Allowability**

Application No.

10/696,159

Examiner

Thao P. Le

Applicant(s)

AMON ET AL.

Art Unit

2818

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--**

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 5/31/05.
2. ☒ The allowed claim(s) is/are 1 and 3-16.
3. ☒ The drawings filed on 31 May 2005 are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) ☐ All   b) ☐ Some\*   c) ☐ None   of the:
    1. ☐ Certified copies of the priority documents have been received.
    2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

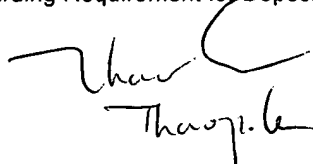
\* Certified copies not received: \_\_\_\_\_.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.  
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
  6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
    - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date \_\_\_\_\_.
    - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date \_\_\_\_\_.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08),  
Paper No./Mail Date \_\_\_\_\_
4. ☐ Examiner's Comment Regarding Requirement for Deposit  
of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413),  
Paper No./Mail Date \_\_\_\_\_
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other \_\_\_\_\_

  
Thao P. Le

## DETAILED ACTION

### Response to Amendment

This Office Action is in response to Amendment filed on 05/31/2005.

Claim 2 has been cancelled.

Claim 1 has been amended.

Claims 1, 3-16 are pending.

Remark of Applicants has been considered.

### Reason for allowance

**Claims 1, 3-16 are allowed.** The following is an examiner's statement of reason for allowance: None of the references of record teaches or suggests the claimed limitations having a method for forming a semiconductor structure having a plurality of gate stacks comprising the steps of forming a sidewall oxide on sidewalls of the gate stacks, and reducing the sidewall oxide in its lateral extend in regions not covered by the mask for resulting in a thinned sidewall oxide after implanting contact doping and among other limitations cited in independent claim 1.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance".

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao P. Le whose telephone number is 571-272-1785. The examiner can normally be reached on M-T (7-6).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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and an overlying second layer made of a metal silicide or a metal.

5 In accordance with a further preferred development, the gate stacks are created by carrying out an application and patterning of the first layer, the overlying second layer and a third layer arranged thereon on the gate dielectric.

10 In accordance with a further preferred development, the third layer has silicon nitride or oxide.

An exemplary embodiment of the invention is illustrated in the drawings and explained in more detail in the  
15 description below.

In the figures:

20 Figures 1A,<sup>1</sup><sub>~</sub>B show a diagrammatic cross-sectional view of a semiconductor structure for elucidating an embodiment of the present invention, figure 1A illustrating a larger detail and figure 1B illustrating the dashed rectangle in figure 1A in an  
25 enlarged view;

Figures 2A,<sup>2</sup><sub>~</sub>B show a diagrammatic cross-sectional view of a semiconductor structure for elucidating successive steps in the  
30 fabrication process in accordance with an embodiment of the present invention; and